IN THE CLAIMS:

Please cancel claims 13 and 14. **Please also amend** claims 1-3 and 7-12 as shown in the complete list of claims that is presented below.

1. (currently amended) A semiconductor integrated circuit comprising:

m scan chains (wherein m is an integer greater than 1) each of which includes a plurality of logic circuits and a plurality of scan registers connected alternately in series, the scan registers being operated in response to a clock signal, each of the scan chains including a first logic circuit having a data input terminal, a first scan register connected to the first logic circuit, the first scan register having a test input terminal, and a last scan register having an output terminal;

a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains, the serial/parallel conversion circuit converting serial data into parallel data in response to a multiplied clock signal having a frequency ~~being~~ that is m times ~~of~~ that of the clock signal; and

a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains, the ~~serial/parallel~~ parallel/serial conversion circuit converting parallel data received from the scan chains into serial data in response to the multiplied clock signal.

2. (currently amended) A semiconductor integrated circuit according to claim 1, further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit, the multiplication circuit receiving the clock signal and generating the multiplied clock signal based on the clock ~~signal~~ signal. ~~received thereto.~~

3. (currently amended) A semiconductor integrated circuit according to claim 1, wherein the serial/parallel conversion circuit ~~including~~ includes a plurality of flip-flops connected in series, the flip-flops being operated in response to the multiplied clock signal.

4. (original) A semiconductor integrated circuit according to claim 1, wherein the parallel/serial conversion circuit including a plurality of flip-flops and a selector, the flip-flops being operated in response to the multiplied clock signal.

5. (currently amended) A semiconductor integrated circuit according to claim 1, wherein each of the ~~serial~~ scan registers includes a selector and a flip-flop ~~being~~ operated in response to the clock signal.

6. (currently amended) A semiconductor integrated circuit according to claim 1, wherein the output terminal of the last scan register of one of the ~~chan~~ scan chains is connected to the data input terminal of the first logic circuit of another one of the scan chains.

7. (currently amended) A semiconductor integrated circuit comprising:

a plurality of scan chains each of which includes a first logic circuit having a data input terminal, a first scan register connected to the first logic circuit, the first scan register having a test input ~~terminal~~ terminal, and a last scan register having an output terminal, the scan registers being operated in response to a clock signal;

a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains, the serial/parallel conversion circuit converting serial data into parallel data in response to a multiplied clock signal having a frequency ~~being a~~ that is substantially equal to the number of ~~times of the~~ scan chains ~~of that~~ times the frequency of the clock signal; and

a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains, the ~~serial/parallel~~ parallel/serial conversion circuit converting parallel data received from the scan chains into serial data in response to the multiplied clock signal.

8. (currently amended) A semiconductor integrated circuit according to claim 7, further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit, the multiplication circuit receiving the

clock signal and generating the multiplied clock signal based on the clock ~~signal~~ signal. ~~received thereto.~~

9. (currently amended) A semiconductor integrated circuit according to claim 7, wherein the serial/parallel conversion circuit ~~including~~ includes a plurality of flip-flops connected in series, the flip-flops being operated in response to the multiplied clock signal.

10. (currently amended) A semiconductor integrated circuit according to claim 7, wherein the parallel/serial conversion circuit ~~including~~ includes a plurality of flip-flops and a selector, the flip-flops being operated in response to the multiplied clock signal.

11. (currently amended) A semiconductor integrated circuit according to claim 7, wherein each of the ~~serial~~ scan registers includes a selector and a flip-flop ~~being~~ operated in response to the clock signal.

12. (currently amended) A semiconductor integrated circuit according to claim 7, wherein the selectors of the ~~serial~~ scan registers are operated in response to a mode signal.

Claim 13-14 (cancelled).